Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A transmission circuit that receives input data at a first rate and outputs data at a second rate, the transmission circuit comprising:

a processor for controlling operations of the transmission circuit, the processor capable of accepting input data and generating corresponding first data having a plurality of bits; and

a format converting circuit electrically connected to the processor for generating second data having a plurality of bits according to the first data, the format converting circuit comprising:

a plurality of input units each for receiving one bit of the first data;

a plurality of output units each for outputting one bit of the second data after receiving the bit; and

a bit control circuit electrically connected between the input units and the output units for generating bits outputted by the output units according to bits received from the input units;the bit control circuit transmitting a bit received by an input unit to an output unit without having the bit passing through other input and output

units, a number of bits between the bit received by the input unit and a most significant bit of the first data being different from a number of bits between the bit outputted by the output unit and a most significant bit of the second data;
wherein the processor further controls the transmission circuit to output data sequentially according to the second data.

[c2] 2.The transmission circuit of claim 1 wherein the processor is capable of buffering the first or second data so that the processor outputs data at a second rate according to the second data.

[c3] 3. The transmission circuit of claim 1 wherein the bit control circuit further comprises an operating circuit electrically connected between the input units and the output units for performing a logical operation according to a predetermined law on the bits received by the input units to generate the bits transmitted by the output units.

[c4] 4. The transmission circuit of claim 1 wherein the bit control circuit further comprises a bit transmission circuit for transmitting a bit of predetermined data to an output unit.

[c5] 5. The transmission circuit of claim 1 wherein the bit control circuit is capable of transmitting two bits received from two different input units to two different output units separately.

[c6] 6. The transmission circuit of claim 1 further comprising a bus connected between the processor and the format converting circuit for transmitting the data between the processor and the format converting circuit.

[c7] 7. A transmission circuit for realizing a rate adaptation layer of a digital communication system, the transmission circuit receiving input data at a first rate and according to the input data generating output data at a second rate, the transmission circuit comprising:
a processor for controlling operations of the transmission circuit, the processor capable of accepting the input data and generating corresponding first data having a plurality of bits; and
a format converting circuit electrically connected to the processor for generating second data according to the first data and a converting control signal from the processor, and transmitting the second data to the processor;
wherein the processor generates an output signal at the second rate according to the second data.

[c8] 8. The transmission circuit of claim 7 wherein the format converting circuit comprises:
a plurality of input units each for receiving one bit of the first data;
a plurality of output units each for outputting one bit of the second data after receiving the bit; and
a bit control circuit electrically connected between the input units and the output units for generating bits outputted by the output units according to bits received from the input units;the bit control circuit transmitting a bit received by an input unit to an output unit without having the bit passing through other input and output units, a number of bits between the bit received by the input unit and a most significant bit of the first data being different from a number of bits between the bit outputted by the output unit and a most significant bit of the second data.

[c9] 9. The transmission circuit of claim 7 wherein the processor is capable of buffering the first or second data so that the processor outputs data at a second rate according to the second data.

[c10] 10. The transmission circuit of claim 7 further comprising a bus connected between the processor and the format converting circuit for transmitting the data between the processor and the format converting circuit.

[c11] 11. The transmission circuit of claim 8 wherein the bit control circuit further comprises an operating circuit electrically connected between the input units and the output units for performing a logical operation according to a predetermined law on the bits received by the input units to generate the bits transmitted by the output units.

[c12] 12. The transmission circuit of claim 8 wherein the bit control circuit further comprises a bit transmission circuit for transmitting a bit of predetermined data to an output unit

13. The transmission circuit of claim 8 wherein the bit control circuit is capable of transmitting two bits received from two different input units to two different output units separately.